Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) In connection with a host processing system capable of delivering commands and raw image data, an apparatus for formatting the raw image data and selectively delivering enhanced image data to a print processing subsystem, said apparatus comprising:

a first interface coupled to said host processing system adapted for receiving said raw image data;

a second interface coupled to said host processing system adapted for receiving said commands, the first interface and the second interface being independent of each other;

a third interface coupled to said print processing subsystem; and

a controller adapted to intercept said raw image data and apply a transformative function to said raw image data to produce enhanced image data and further to cause said enhanced image data to be delivered to said print processing subsystem via said third interface.

2. (Original) The apparatus according to Claim 1 wherein said first interface is an image bus interface adapted to transmit said raw image data.

3. (Original) The apparatus according to Claim 2 wherein said image bus interface is further identified as a special bus write function.

4. (Original) The apparatus according to Claim 1 wherein said host processing system is selected from the group consisting of a Pentium™ processor, a Power Personal Computer (PC) type processor, and a Crusoe™ processor.

5. (Original) The apparatus according to Claim 1 further comprising a front end memory coupled to said first interface, said front end memory adapted to receive said raw image data.

6. (Original) The apparatus according to Claim 5 further comprising back end memory communicably coupled to said front end memory, said back end memory adapted to receive said enhanced image data.

7. (Original) The apparatus according to Claim 6 wherein said front end memory and said back end memory are Random Access Memory (RAM).

8. (Original) The apparatus according to Claim 6 wherein said third interface is a printer interface coupled to said back end memory, said printer interface adapted to transmit print data based on said enhanced image data to said print processing subsystem.

9. (Original) The apparatus according to Claim 1 further comprising a processor adapted to receive processing instructions from said host processing system and transmit said processing instructions to said host processing system.

10. (Original) The apparatus according to Claim 9 wherein said processing instructions include initialization commands, error information, diagnostic information, bad nozzle data for failed nozzle correction, and other instructions for processing a print job.

11. (Original) The apparatus according to Claim 9 wherein said second interface is a processor bus interface coupled to said host processing system, said processor bus interface adapted to communicate said processing instructions between said processor and said host processing system.

12. (Original) The apparatus according to Claim 9 further comprising a gateway communicably coupling said processor to said front end memory and said back end memory whereby said processor formats said raw image data as read out of said front end memory, and transmits said enhanced image data to said back end memory.

13. (Original) The apparatus according to Claim 12 further comprising:

an image data bus coupling said first interface to said front end memory; and

a first local bus coupling said second interface to said processor;

wherein said gateway communicably couples said image data bus and said first local bus.

14. (Original) The apparatus according to Claim 13 further comprising:

a control data buffer coupled to said first local bus;

a low speed communications device in communication with said control data buffer; and

a second local bus coupling said control data buffer and said low speed communications device.

15. (Original) The apparatus according to Claim 14 wherein said control data buffer is a bus transceiver and said low speed communications device is a debug serial port.

16. (Original) The apparatus according to Claim 9 wherein said processor is an image processor.

17. (Original) The apparatus according to Claim 10 further comprising Read Only Memory (ROM) containing an image processing control program coupled to said image processor.

18. (Original) The apparatus according to Claim 10 further comprising Random Access Memory (RAM) coupled to said image processor and serving as a workspace for formatting by said image processor.

19. (Currently Amended) A device for formatting raw image data and selectively delivering enhanced image data to a print processing subsystem, said device comprising:

an image data bus section having an image bus interface adapted to be coupled to a host processing system to transmit the raw image data, a front end memory coupled to said image bus interface to receive said raw image data, a back end memory for receiving said enhanced image data, and a print interface coupled to said back end memory for transmitting print data based on said enhanced image data as read out of said front end memory and transmitting the enhanced image data to said print processing subsystem;

a processor bus section having an image processor, a processor bus interface adapted to be coupled to said host processing system to communicate print processing instructions between said image processor and said host processing system, the processor bus interface being independent of the image bus interface, the processor bus interface and the image bus interface operating in parallel; and

a gateway coupling said image processor to said front end memory and said back end memory whereby said image processor formats said raw image data and transmits said enhanced image data to the back end memory.

20. (Original) The device according to Claim 19 wherein said image bus interface is identified as a special bus write function.

21. (Original) The device according to Claim 19 wherein handshaking between said image processor and said host processing system is accomplished through said processor bus interface.

22. (Original) The device according to Claim 19 further comprising Read Only Memory (ROM) containing an image processing control program coupled to said image processor.

23. (Original) The device according to Claim 19 further comprising Random Access Memory (RAM) coupled to said image processor and serving as a workspace for formatting said raw image data by said image processor.

24. (Original) The device according to Claim19 further comprising:

an image data bus coupling said image bus interface to said front end memory; and

a local bus coupling said processor bus interface to said image processor;

wherein said gateway couples said image data bus and said local bus.

25. (Original) The device according to Claim 19 wherein said print interface is adapted to output data to a plurality of printheads via said print processing subsystem.

26. (Original) An apparatus as recited in Claim 24 further comprising a buffer coupled to said local bus and a low speed communications device coupled to said buffer.

27. (Currently Amended) A method for formatting bitmapped image data comprising the steps of:

transmitting raw image data, through an image bus interface coupled to a host processing system, to a front end memory coupled to the image bus interface for receiving said raw image data;

communicating print processing instructions, through a processor bus interface coupled to said host processing system, to an image processor, the processor bus interface being independent of the image bus interface, the processor bus interface and the image bus interface connected in parallel to the host processing system;

transferring said raw image data from the front end memory to the print processor through a gateway coupling the print processor to the front end memory;

formatting the raw image data via said image processor;

transferring enhanced image data to a back end memory;

reading said enhanced image data out of said back end memory; and

transmitting said enhanced image data readout from the back end memory to a print processing subsystem via a print interface.

28. (Original) The method according to Claim 27 further comprising the step of identifying the image bus interface as a special bus write function.

29. (Original) The method according to Claim 28 further comprising the step of accomplishing handshaking between the image processor and said host processing system through the processor bus interface.

30. (Original) The method according to Claim 27 further comprising the step of downloading control instructions from a Read Only Memory (ROM) to the image processor.

31. (Original) The method according to Claim 27 further comprising the step of receiving command instructions from a second local bus.

32. (Original) The method according to Claim 27 wherein said formatting step includes the step of utilizing a Random Access Memory (RAM) coupled to the image processor as a workspace.

33. (Original) The method according to Claim 27 further comprising the step of dividing said enhanced image data into data for a plurality of printheads in said print interface.

34. (Original) The method according to Claim 27 wherein said step of transmitting said enhanced image data readout from the back end memory to a print processing subsystem via a print interface is followed by the step of delivering said enhanced image data to a plurality of printheads.

35-40 (Cancel)

41. (New) The apparatus according to Claim 1 wherein the first bus is used for transmission of image data signals from the host processing system.

42. (New) The apparatus according to Claim 41 wherein the second bus is used for transmission of processor instruction signals from the host processing system.